## REMARKS/ARGUMENTS

### INFORMATION DISCLOSURE STATEMENT

First, the Examiner noted that that IDS submitted on January 8, 2002 was not considered because the references were not in the file. Accordingly, Applicants have resubmitted the IDS with this Amendment and Response, and request that the Examiner consider the cited references.

### STATUS OF THE APPLICATION

Prior to this amendment, claims 1 - 19 were pending in this application. The Examiner objected to claim 5 because it included a typographical error. In addition, the Examiner rejected claims 16-19 under 35 U.S.C. § 102(b) as being anticipated by Hagersten et al., U.S. Patent No. 5,710,907 (hereinafter "Hagersten"). Finally, the Examiner rejected claims 1-15 under 35 U.S.C. § 103(a) as being unpatentable over Hagersten in view of Hsu et al, U.S. Patent No. 6,128,700 (hereinafter "Hsu").

Applicants have amended claims 1 and 5. Claims 2-4 and 6-19 remain unchanged. Applicants submit that no new subject matter has been introduced by these amendments. Claims 1-19 remain pending in this application after filing this amendment.

### THE CLAIMS

Claim Objections

The Examiner objected to claim 5 because it contains a typographical error. Applicants have amended claim 5 to fix the error. Accordingly, Applicants submit that claim 5 now is in condition for allowance.

Section 102(b) Rejections

The Examiner has rejected claims 16-19 under 35 U.S.C. § 102(b) as being anticipated by Hagersten. Applicants disagree with the Examiner's rejection, and therefore,

traverse the rejection. Applicants respectfully submit the following arguments in support of their position.

Hagersten discloses a hybrid Non-Uniform Memory Architecture (NUMA) and Cache-Only Memory Architecture (COMA) caching architecture together with a cache-coherent protocol for a computer system having a plurality of sub-systems coupled together via a system interconnect. Each sub-system (310, 320, ..., 380) includes one or more processors, corresponding memory management units (MMUs), corresponding hybrid second level cache (L2$s), a COMA cache memory, a global interface, an address translator, a directory table and local interconnect. (Col. 8, Lines 63-67). In each subsystem, each of the plurality of processors is connected to a corresponding MMU which is connected to memory. (Fig. 3A, Col. 9, Lines 8-16). This is a standard configuration for a computer system or subsystem. Hagersten, however, does not teach that these components of a computer system are fabricated on a single processor chip as recited in the claims. Indeed, independent claim 16 recites:

> In a computer architecture having a plurality of processor chips, each comprising a processing core and at least one bank of memory, a method for a first processing core on a first processor chip of accessing said at least one bank of memory on a second processor chip, comprising the steps of:
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> said first processing core on said first processor chip issuing a memory request;
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> determining whether said memory request is accessing data in said at least one bank of memory on said first processor chip or data in said at least one bank of memory on said second processor chip;
>
> if said memory request is accessing data in said at least one bank of memory on said second processor chip, communicating said memory request to said second processor chip;
>
> performing a memory access function to said at least one bank of memory on said second processor chip; and
>
> communicating a result of said memory access function back to said first processing chip.
>
> (emphasis added).

In the invention recited in independent claim 16, each processor chip includes a processing core and at least one bank of memory. Hagersten does not disclose a processor and memory fabricated on a single chip. Indeed, the subsystems disclosed in Hagersten include multiple processors with multiple MMUs and multiple banks of memory interconnected via a local interconnect. This configuration could not be fabricated on a single chip as recited in claim 16, particularly in 1995 when Hagersten was filed. Thus, the subsystems disclosed in Hagersten, at best, comprise multiple chips connected on a circuit board. In fact, the subsystems in Hagersten probably comprise multiple circuit boards, or separate computers connected via communication interconnects. Regardless of the configuration of the subsystems of Hagersten, it is apparent from the disclosure, as well as the state of the art at that time that Hagersten does not disclose a processor chip including a processing core and at least one bank of memory, and Hagersten does not disclose a plurality of these processor chips communicating in the manner recited in claim 18. As a result, Applicants respectfully submit that claim 16 is patentable over Hagersten.

With regard to dependent claims 17-19, Applicants submit that these claims are allowable as being directed to specific novel substitutes, as well as by depending from allowable parent claims.

Section 103(a) Rejections

The Examiner has rejected claims 1-15 under 35 U.S.C. § 103(a) as being unpatentable over Hagersten in view of Hsu. Again, Applicants disagree with the Examiner's rejection, and therefore, traverse the rejection. Applicants respectfully submit the following arguments in support of their position.

With regard to claim 1, Applicants have amended the claim so that it now recites:

> A processor chip, comprising:
>
> a processing core; and
>
> at least one bank of DRAM memory, including a mode control input for controlling the mode of said at least one bank of DRAM memory between a first mode and a second mode, wherein when said at least one bank of DRAM memory is in said first mode, said at least one bank of DRAM memory acts as physical

memory, and when said at least one bank of DRAM memory is in said second mode, said at least one bank of DRAM memory acts as cache memory;

wherein the processing core and the at least one bank of DRAM memory are fabricated on a single processor chip.

(emphasis added).

As discussed in detail above, Hagersten does not disclose a processing core and at least one bank of DRAM memory fabricated on a single processor chip. Further, Hsu also does not disclose this limitation. Indeed, all Hsu discloses is the use of DRAM as a second level cache memory. Nowhere does it discuss fabricating the DRAM on the same chip as the processing core. As a result, Applicants submit that independent claim 1 is allowable over the cited references.

With regard to dependent claims 2-7, Applicants submit the these claims are allowable as being directed to specific novel substitutes, as well as by depending from allowable parent claims.

With regard to independent claim 8, it recites:

In a computer system, a scalable computer processing architecture, comprising:

one or more processor chips, each comprising:

a processing core;

at least one bank of DRAM memory including a mode control input for controlling the mode of said at least one bank of DRAM memory between a first mode and a second mode, wherein when said at least one bank of DRAM memory is in said first mode, said at least one bank of memory acts as physical memory, and when said at least one bank of DRAM memory is in said second mode, said at least one bank of DRAM memory acts as cache memory;

an I/O link configured to communicate with other of said one or more processor chips or with I/O devices;

a communication and memory controller in electrical communication with said processing core, said at least one bank of memory, and said I/O link;

> said communication and memory controller for controlling the exchange of data between said one or more processor chips and I/O devices, and for receiving memory requests from said processing cores on said one or more processor chips and from said I/O devices, and processing said memory requests with said at least one bank of memory.
>
> wherein said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said I/O links of said processor chips, so as to create multiple processing core pipelines which share data therebetween.

In this claim, a processing core, at least one bank of DRAM memory, an I/O link, a communications and memory controller all are configured on a single processor chip. Further, the claim recites that two or more processor chips can be connected in parallel via the I/O links. As explained above, neither Hegersten nor Hsu disclose anything close to this. Thus, Applicants respectfully submit that independent claim 8 also is allowable over the cited references.

Finally, with respect to dependent claims 9-15, Applicant submit that these claims are allowable as being directed to specific novel substitutes, as well as by depending from allowable parent claims.

## CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. Accordingly, Applicants respectfully request the Examiner to issue a formal Notice of Allowance as soon as possible.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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